Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (presently amended) A method, comprising:

by a memory controller:

for a first read of information from a memory, activating termination loads on said memory controller's side of a data bus between said memory controller and said memory, said activating being a consequence of a first signal's indication of a first clock cycle of a plurality of consecutive clock cycles, a memory read phase being performed by said memory controller over said plurality of clock cycles, said first read of information occurring within said plurality of clock cycles;

for a write of information into said memory, deactivating said termination loads; and,

for a second read of information from said memory, activating said termination loads.

2. (canceled).

3. (original) The method of claim 2 further comprising, by said memory controller, imposing a programmed delay to said first signal to create a second delayed signal and triggering said activating of termination loads from said second signal.

4. (original) The method of claim 3 wherein said triggering further comprises latching a logic value from said second signal, said logic value provided to said termination loads to cause their activation.

5. (original) The method of claim 2 further comprising triggering said activating of said termination loads by latching a logic value in response to said first signal's indication, said logic value provided to said termination loads to cause their activation.

6. (original) The method of claim 5 further comprising latching a second logic value in response to a second signal, said second logic value provided to said termination loads to cause their deactivation for said write of information.

7. (original) The method of claim 2 wherein said first signal is a chip select (CS) signal.

8. (original) The method of claim 1 wherein said deactivating occurs within a clock cycle that immediately follows a last clock cycle of a plurality of clock cycles that mark a read phase within which said first read of information occurs.

9. (original) The method of claim 1 wherein said activating occurs in response to an edge that appears in a chip select (CS) signal.

10. (original) The method of claim 1 further comprising asserting a bypass control signal to activate said termination loads while information is being read from said memory.

11. (original) The method of claim 1 further comprising asserting an enable control signal and not asserting a bypass control signal so as to permit said activating.

12. (original) The method of claim 1 further comprising:

by said memory controller:

for said first read of information from a memory, activating a termination load on said memory controller's side of a data strobe wire between said memory controller and said memory;

for said write of information into said memory, deactivating said data strobe wire's said termination load; and,

for said second read of information from said memory, activating said data strobe wire's termination load.

13. (presently amended) An apparatus, comprising:

a memory controller comprising a data bus's termination loads, said data bus to couple to a memory, said termination loads coupled to an output of memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said termination loads in an activated state during a memory read phase and to place said termination loads in a deactivated state

during a memory write phase, said memory controller logic circuitry comprising a latch, said latch to latch a first value, said first value to place said termination loads in said activated state, said latch to also provide a second value, said second value to place said termination loads in said deactivated state.

14. (canceled).

15. (original) The apparatus of claim 14 wherein said second value corresponds to a response to a clear input of said latch being activated.

16. (original) The apparatus of claim 13 wherein said logic circuitry further comprises a logic gate between said output and a bypass input to said logic circuitry, said logic gate to place said termination loads into one of said states when said bypass input is asserted.

17. (original) The apparatus of claim 13 wherein said logic circuitry further comprises a second logic gate between said output and a tweak input, said second logic gate to place said termination loads into said activated state based upon a first tweak input value, said second logic gate to place said termination loads into said deactivated state based upon a second tweak input value.

18. (original) The apparatus of claim 13 wherein said logic circuitry further comprises a chain of delay elements to allow a delay to be programmed, said delay imposed between a first moment when a memory read phase is indicated and a second following moment when said termination loads are placed into said activated state.

19. (original) The apparatus of claim 13 wherein said memory controller further comprises a data strobe wire's termination load, said data strobe wire to couple to said memory, said data strobe wire's termination load coupled to said output of said memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said data strobe wire's termination load in an activated state during said memory read phase and to place said data strobe's termination load in a deactivated state during said memory write phase.

20. (presently amended) A method, comprising:

by a computing system:

for a first read of information from a DDR memory, activating termination loads on said memory controller's side of a data bus between said memory controller and said DDR memory, said activating being a consequence of a first signal's indication of a first clock cycle of a plurality of consecutive clock cycles, a DDR memory read phase being performed by said memory controller over said plurality of clock cycles,

said first read of information occurring within said plurality of clock cycles;

for a write of information into said DDR memory, deactivating said termination loads; and,

for a second read of information from said DDR memory, activating said termination loads.

21. (canceled).

22. (original) The method of claim 21 further comprising, by said memory controller, imposing a programmed delay to said first signal to create a second delayed signal and triggering said activating of termination loads from said second signal.

23. (original) The method of claim 22 wherein said triggering further comprises latching a logic value from said second signal, said logic value provided to said termination loads to cause their activation.

24. (original) The method of claim 21 further comprising triggering said activating of said termination loads by latching a logic value in response to said first signal's indication, said logic value provided to said termination loads to cause their activation.

25. (original) The method of claim 24 further comprising latching a second logic value in response to a second signal, said second logic value provided to said termination loads to cause their deactivation for said write of information.

26. (original) The method of claim 21 wherein said first signal is a chip select (CS) signal.

27. (original) The method of claim 20 wherein said deactivating occurs within a clock cycle that immediately follows a last clock cycle of a plurality of clock cycles that mark a read phase within which said first read of information occurs.

28. (original) The method of claim 20 wherein said activating occurs in response to an edge that appears in a chip select (CS) signal.

29. (original) The method of claim 20 further comprising asserting a bypass control signal to activate said termination loads while information is being read from said DDR memory.

30. (original) The method of claim 20 further comprising asserting an enable control signal and not asserting a bypass control signal so as to permit said activating.

31. (original)The method of claim 20 further comprising:

by said memory controller:

for said first read of information from a DDR memory, activating a termination load on said memory controller's side of a data strobe wire between said memory controller and said DDR memory;

for said write of information into said DDR memory, deactivating said data strobe wire's termination load; and,

for said second read of information from said DDR memory, activating said data strobe wire's termination load.

32. (presently amended) An apparatus, comprising:

a computing system comprising:

a memory controller comprising a data bus's termination loads, said data bus coupled to a DDR memory, said termination loads coupled to an output of memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said termination loads in an activated state during a read phase of said DDR memory and to place said termination loads in a deactivated state during a write phase of said DDR memory, said memory controller logic circuitry comprising a latch, said latch to latch a first value, said first value to place said termination loads in said activated state, said latch to also provide a second value, said second value to place said termination loads in said deactivated state.

33. (canceled).

34. (original) The apparatus of claim 33 wherein said second value corresponds to a response to a clear input of said latch being activated.

35. (original) The apparatus of claim 32 wherein said logic circuitry further comprises a logic gate between said output and a bypass input to said logic circuitry, said logic gate to place said termination loads into one of said states when said bypass input is asserted.

36. (original) The apparatus of claim 32 wherein said logic circuitry further comprises a second logic gate between said output and a tweak input, said second logic gate to place said termination loads into said activated state based upon a first tweak input value, said second logic gate to place said termination loads into said deactivated state based upon a second tweak input value.

37. (original) The apparatus of claim 32 wherein said logic circuitry further comprises a chain of delay elements to allow a delay to be programmed, said delay imposed between a first moment when a read phase of said DDR memory is indicated and a second following moment when said termination loads are placed into said activated state.

38. (original) The apparatus of claim 13 wherein said memory controller further comprises a data strobe wire's termination load, said data strobe wire to couple to said DDR memory, said data strobe wire's termination load coupled to said output of

said memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said data strobe wire's termination load in an activated state during said DDR memory read phase and to place said data strobe's termination load in a deactivated state during said DDR memory write phase.

39. (presently amended) A machine readable medium having stored thereon a description of a design for a memory controller, the memory controller comprising:

a data bus's termination loads, said data bus to couple to a memory, said termination loads coupled to an output of memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said termination loads in an activated state during a memory read phase and to place said termination loads in a deactivated state during a memory write phase, said memory controller logic circuitry comprising a latch, said latch to latch a first value, said first value to place said termination loads in said activated state, said latch to also provide a second value, said second value to place said termination loads in said deactivated state.

40. (deleted).

41. (original) The machine readable medium of claim 40 wherein said second value corresponds to a response to a clear input of said latch being activated.

42. (original) The machine readable medium of claim 39 wherein said logic circuitry further comprises a logic gate between said output and a bypass input to said logic circuitry, said logic gate to place said termination loads into one of said states when said bypass input is asserted.

43. (original) The machine readable medium of claim 39 wherein said logic circuitry further comprises a second logic gate between said output and a tweak input, said second logic gate to place said termination loads into said activated state based upon a first tweak input value, said second logic gate to place said termination loads into said deactivated state based upon a second tweak input value.

44. (original) The machine readable medium of claim 39 wherein said logic circuitry further comprises a chain of delay elements to allow a delay to be programmed, said delay imposed between a first moment when a memory read phase is indicated and a second following moment when said termination loads are placed into said activated state.